Notice of References Cited Application/Control No. 10/709,293 Examiner Suchin Parihar Applicant(s)/Patent Under Reexamination ALLEN ET AL. Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	Α	US-6,738,954	05-2004	Allen et al.	716/4
*	В	US-2004/0096092	05-2004	Ikeda, Takahiro	382/141
*	С	US-2005/0108669	05-2005	Shibuya, Toshiyuki	716/009
*	D	US-2005/0021234	01-2005	Han, Dianli	702/013
*	E	US-2005/0168731	08-2005	Shibuya et al.	356/237.4
*	F	US-6,948,141	09-2005	Satya et al.	716/4
	G	US-			
•	Н	US-			
		US-			_
	J	US-			
	K	US-			
	L	US-			·
	М	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	0					
	P					
	Q					
	R					
	S				.,	
	Т					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)						
	U	E. Papadopoulou and D. T. Lee, "Critical area computation via voronoi diagrams," IEEE Trans. Computer-Aided Design, vol. 18, pp. 463-474, Apr. 1999.						
	V	[7] E. Papadopoulou, "Critical area computation for missing material defects in VLSI circuits," IEEE Trans. Semiconduct. Manufact., vol. 20, pp. 583-597, May 2001.						
	W	E. Papadopoulou, D.T. Lee, "Critical Area Computation - A new Approach", Proc. International Symposium on Physical Design, April 1998, 89-94.						
	×							

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).) Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.